LAIKIPIA UNIVERSITY

UNIVERSITY EXAMINATIONS

SECOND SEMESTER 2023/2024 ACADEMIC YEAR

FOURTH YEAR EXAMINATION FOR THE DEGREE BACHELOR OF EDUCATION (SCIENCE) AND BACHELOR OF SCIENCE (GENERAL)

PHYS 422: DIGITAL ELECTRONICS

STREAM: R ***TIME: 2 HRS***

DAY: TUESDAY[2.30P.M -4.30P.M] ***DATE: 16/04/2024***

THIS QUESTION PAPER CONSISTS OF FIVE (5) PAGES

PLEASE DO NOT OPEN UNTIL THE INVIGILATOR SAYS SO.

INSTRUCTIONS:

- Read the question paper carefully.
- Answer Question ONE and any other TWO Questions.
- Question **ONE** carries **40 marks** and the other **FOUR** carry **15 marks** each.
- Do not carry mobile phones or any electronic transmission device to the examination room.

QUESTION ONE (40 MARKS)

(a) Define the following terms as used in Digital Electronics:

(i) Code

(ii) Bit

(iii) Digitization **(3 Marks)**

(b) (i) Verify that a two level AND – OR topology is equivalent to a NAND – NAND system **(4 Marks)**

(ii) Convert the decimal number 274.1875 to their binary equivalent. **(4 Marks)**

(iii) Convert the hexadecimal number $7C9_{16}$ to their decimal equivalents: **(2 Marks)**

(c) Give two advantages of digital signals **(2 Marks)**

(d) Solve the following in Hexadecimal

(i) 0300 - 005A

(ii) 91B +6F2 **(4 Marks)**

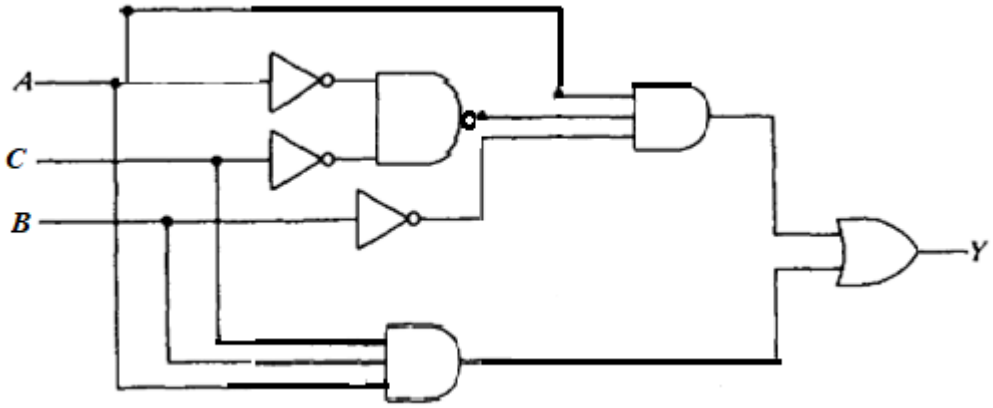
(e) Adopt a 6 bit notation to perform arithmetic operations of the following decimal numbers in Binary, and confirm the answer

(i) 24 + 26 (ii) +9 - 13 (iii) -5 -13 **(6 Marks)**

(f). Use J-K flip flops and other relevant logic gates to design an asynchronous decade counter. How would the circuit of the asynchronous decade counter be modified into a synchronous decade counter? **(6 Marks)**

(g). What are the advantages of digital signals over analog signals? **(3 Marks)**

(h). (i) Simplify the logic circuit shown below. **(4 Marks)**



(ii) Draw the logic diagram of the simplified circuit in (i) above using NAND gates only.

(2 Marks)

QUESTION TWO (15 MARKS)

(a) Convert the binary number 11111001100 to its equivalent decimal number **(3 Marks)**

(b) A person claims to be born in $7C8_{hex}$ year. What is his actual age in binary and decimal systems? **(4 Marks)**

(c) Convert the following Boolean expression into standard POS form:

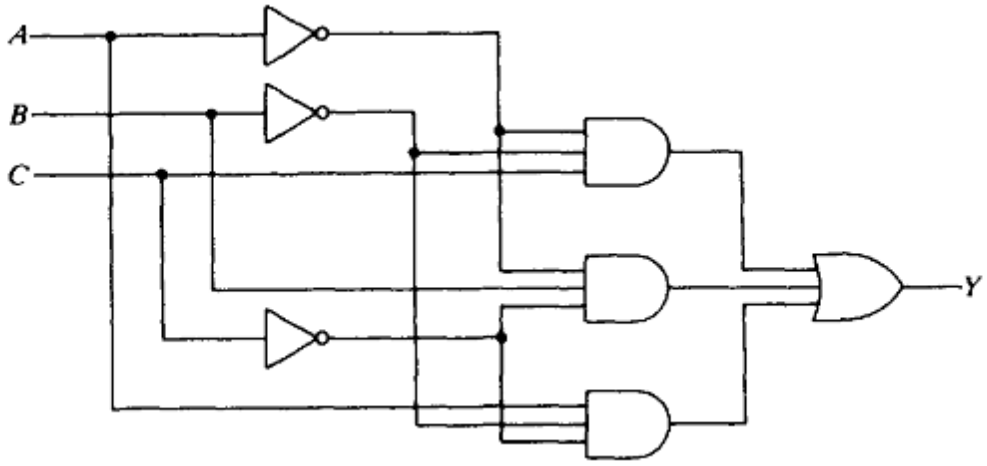
$$(A + \bar{B} + C)(\bar{B} + C + \bar{D})(A + \bar{B} + \bar{C} + D)$$ **(5 Marks)**

(d) Use the Karnaugh map to minimize the following standard SOP expression:

$$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$ **(3 Marks)**

QUESTION THREE (15 MARKS)

(a) Consider the logic gate circuit diagram below.



(i) Write the Boolean expression for the logic circuit **(2 Marks)**

(ii) Obtain the truth table in binary numbers for the logic circuit **(3 Marks)**

(b) Determine the binary values of the variables for which the following standard SOP expression is equal to zero $(A + B + C + D)(A + \bar{B} + \bar{C} + D)(\bar{A} + B + \bar{C} + \bar{D})$ **(4 Marks)**

(c) Show how a computer would multiply the binary numbers 1001 and 1011 which are in 2's compliment. Assume MSB is a sign bit. **(3 Marks)**

(d) (i) Differentiate between an Excess-3 code and a Gray- code. **(1 Mark)**

(ii) Convert the following binary numbers to Gray- code (a). 110100 (b). 101101 **(2 Marks)**

QUESTION FOUR (15 MARKS)

(a) Draw the logic circuit represented by the expression Y= $A\bar{B}C + AB\bar{C}$ **(2 Marks)**

(b) Given the expression: Y = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}\bar{B}\bar{C} + AB\bar{C}$. Obtain a minimized expression using K-map **(3 Marks)**

(c) (i). Differentiate between SRAM and DRAM **(2 Marks)**

(ii). What is the advantage of a computer with many registers over the one with few **(1 Mark)**

(iii). Define an analogue signal **(1 Mark)**

(d). Draw a labelled block diagram of a complete 4-bit parallel adder with registers capable of ADD and SUBTRACT operations. **(6 Marks)**

QUESTION FIVE (15 MARKS)

(a) Using NAND gates draw a logic symbol of a clocked SR flip-flop. Briefly explain the operation of the clocked SR flip-flop. **(6 Marks)**

5. (b). (i). The waveforms in Fig. 1 are applied to the J, K, in Fig. 2 and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET. (**5 Marks**)

Fig.

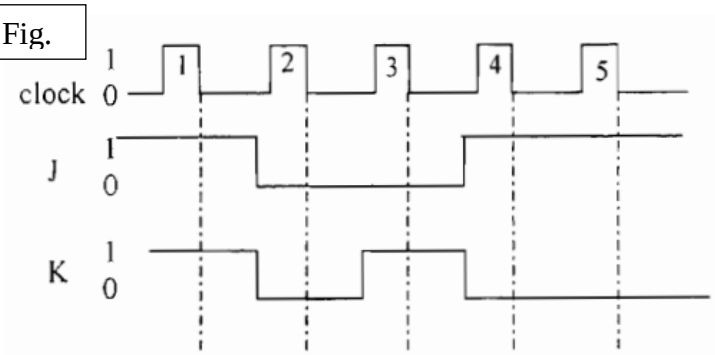
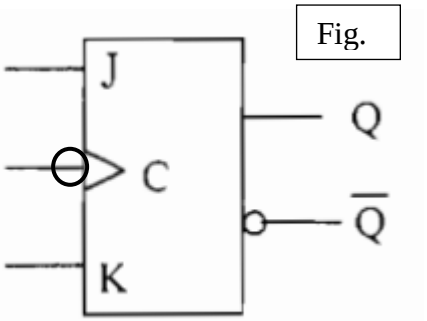
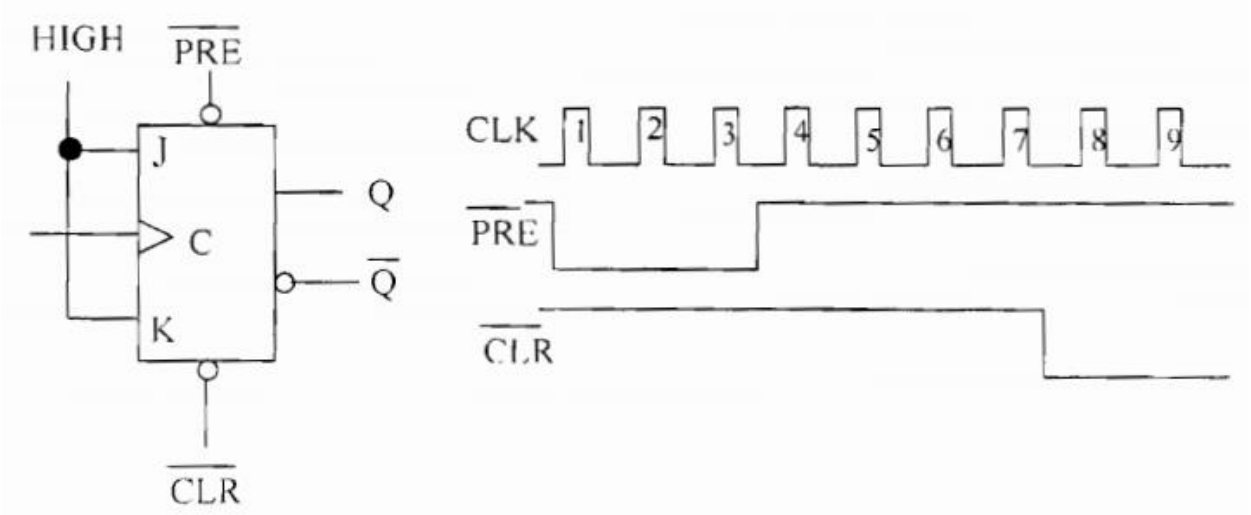


Fig.



5. (b). (ii). For the positive edge triggered J-K flip flop with preset and clear inputs in the Figure below, determine the Q output for the inputs shown in the timing diagram if Q is initially LOW.



(4 Marks)